REMARKS/ARGUMENTS

Claims 1-27 are pending in the present application. By this response, claims 1, 5, 9, 10, 18, 19 and 27 are amended, claims 8, 17, and 26 are canceled, and claims 28-30 are added. Support for the amendments to claims 1, 5, 9, 10, 18, and 27 can be found in the claims as originally filed. Support for the amendment to claim 19 can be found at least in the Specification at page 17. Support for new claims 28-30 can be found at least in the Specification at pages 7 and 8. Reconsideration of the claims is respectfully requested.

I. Interview Summary

An interview was held with the Examiner on August 24, 2006. During the course of the interview, the Examiner approved Applicants proposed changes to claims 5 and 19 in order to overcome the Examiner's 112 and 101 rejections, respectively. No agreement was reached with respect to the anticipation rejection.

II. Objection to the Claims

The Examiner stated that claims 9, 18, and 27 are objected to because of the following informalities: "Per claims 9, 18, and 27, the acronym 'TCE' should be spelled out as "Translation Control Entry" as the acronym is first mentioned in these claims." Applicants have amended the claims accordingly. Therefore, the objection to the claims has been overcome.

III. 35 U.S.C. § 112, Second Paragraph

The Examiner rejected claim 5 under §112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. In response, Applicants have amended dependent claim 5 in the manner approved by the Examiner during the 8/24/06 interview. Accordingly, the rejection of claim 5 under §112, second paragraph, has been overcome.

IV. 35 U.S.C. § 101

The Examiner rejected claims 19-27 as directed towards non-statutory subject matter. In response, Applicants have amended independent claim 19 in the manner approved by the Examiner during the 8/24/06 interview. Accordingly, the rejection of claim 19 under §101 has been overcome. Furthermore, because the Examiner rejected dependent claims 20-27 on the basis of their dependency on claim 19, the rejection of claims 20-27 has also been overcome.

V. Asserted Anticipation under 35 U.S.C. § 102

The Examiner rejected claims 1-3, 5, 6, 8, 10-12, 14, 15, 17, 19-21, 23, 24, and 26 as anticipated by *Dawkins et al.*, Method and Apparatus to Power Off and/or Reboot Logical Partitions in a Data Processing System, U.S. Patent Application Publication 2002/0124194 A1 (March 21, 2001) (hereinafter "*Dawkins*"). This rejection is respectfully traversed.

V.A. Asserted Anticipation of the Independent Claims

Regarding claims 1, 10, and 19, the Examiner states:

> **Per claims 1, 10 and 19**, Dawkins teaches a method in a data processing system for providing valid translation entries in a translation control entry table (TCE facility and TCE Table, see Pg. 4, Para. [0043], [0044], [0046]) for all supported direct memory addresses, comprising:
>
> reserving a page in system memory ("a reserved page per image ... ", see Pg. 4, Para. [0046]);
>
> writing the reserved page (a page of memory is written to when a write operation from the operating systems addresses a memory range within the page);
>
> selecting a region in system memory for the translation control entry table (the TCE table must be stored somewhere in system memory for the Hypervisor and the operating systems to access it, see Pg. 4, Para. [0046]); and
>
> initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page ("initializes all entries in ... TCE table to point to a reserved page ... ", see Pg. 4, Para. [0044] and [0046]).
>
> It is also clear the data processing system of claim 10 is already substantially disclosed above, as well as the computer program product ("software", see Pg. 5, Para. [0050] and [0051]; "computer instructions", see Pg. 6, Para. [0066], [0068] and [0076]) of claim 19.)

Office Action dated June 6, 2006, p. 4.

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Dawkins fails to anticipate independent claims 1, 10, and 19 because *Dawkins* does not teach each and every element recited in claims 1, 10, and 19. Independent claim 1 is as follows:

1. A method in a data processing system for providing valid translation entries in a translation control entry table for all supported direct memory addresses, comprising:

reserving a page in system memory;

writing the reserved page;

selecting a region in system memory for the translation control entry table; and

initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page.

Specifically, *Dawkins* does not anticipate claim 1 because *Dawkins* does not teach "writing the reserved page" and "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page."

In discussing the anticipation of "writing the reserved page," the Examiner fails to particularly point out any portion of *Dawkins* that teaches this feature. Instead, the Examiner states only that "a page of memory is written to when a write operation from the operating systems addresses a memory range within the page." This assertion does not describe how *Dawkins* teaches the claim feature at issue. In fact, *Dawkins* does not anywhere actually teach "writing the reserved page," as recited in claim 1.

The Examiner also asserts that *Dawkins* teaches the feature "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page" in paragraph 0044, reproduced above. However, paragraph 0044 of *Dawkins* only teaches the manner in which the TCE table and the I/O bus provide bits to access memory. For example, TCE bits determine which page in the memory is addressed, and the bits from the I/O bus determine the address within the page.

In contrast, paragraph 44 of *Dawkins* does not teach "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page." Although *Dawkins's* TCE table contains the addresses of the reserved pages, the page entries in the TCE table are not also *initialized to be valid* as recited in claim 1. For this reason, paragraph 44 does not teach the "initializing" feature of claim 1.

The Examiner also alleges that *Dawkins* teaches this "initializing" feature of claim 1 in paragraph 0046, reproduced below:

> [0046] When platform 400 is initialized, a disjoint range of I/O bus DMA addresses is assigned to each of I/O adapters 448-462 for the exclusive use of the respective one of I/O adapters 448-462 by hypervisor 410. Hypervisor 410 then configures the terminal bridge range register (not shown) facility to enforce this exclusive use. Hypervisor 410 then communicates this allocation to the owning one of OS images 402-408. Hypervisor also initializes all entries in a particular I/O adapter's associated section of the TCE table to point to a particular reserved page per image that is owned by the OS image that is allocated to that I/O

adapter, such that unauthorized accesses to memory by an I/O adapter will not create an error that could affect one of the other OS images 402-408.

Paragraph 46, however, only teaches a hypervisor that assigns bus DMA addresses for the exclusive use by the I/O adapters, and then communicates this allocation to the OS images. The hypervisor initializes the entries of the TCE table *to point to a particular reserved page allocated to the I/O adapters*. Without verifying that the reserved page is actually valid, a subsequent DMA translation may still result in an unrecoverable error. Thus, paragraph 46 does not teach "initializing all entries in the translation control entry table, *wherein all entries are initialized to be valid*," as recited in claim 1. Accordingly, *Dawkins* does not anticipate claim 1 because *Dawkins* fails to teach each and every feature of claim 1.

In addition, during the course of the Examiner interview, the Examiner admitted that *Dawkins* fails to disclose the step "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page." The Examiner believes that this feature is inherently disclosed by *Dawkins*. The Examiner, however, has misapplied the concept of "inherent" anticipation.

Section 102 of Title 35 deals with novelty and loss of patent rights. An invention is said to be "anticipated" when it is squarely described or disclosed in a single reference as identified from one of the categories of 35 U.S.C. §102, commonly referred to as "prior art". Express anticipation occurs when the invention is expressly disclosed in the prior art, patent or publication. In some cases, however, when the claimed invention is not described *in haec verba*, the "doctrine of inherency" is relied on to establish anticipation. Under the principles of inherency, a claim is anticipated if a structure in the prior art ***necessarily*** functions in accordance with the limitations of a process or method claim. *In re King*, 801 F.2d 1324, 231 U.S.P.Q. 136 (Fed. Cir. 1986). A prior art reference that discloses all of a patent's claim limitations anticipates that claim even though the reference does not expressly disclose the "inventive concept" or desirable property the patentee discovered. *Verdgaal Brothers, Inc. v. Union Oil Company of California*, 814 F.2d 628, 2 U.S.P.Q.2d 1051, (Fed. Cir. 1987). It suffices that the prior art process inherently possessed at that property. *Id.* ***Mere possibilities or even probabilities, however, are not enough to establish inherency.*** The missing claimed characteristics must be a "natural result" flowing from what is disclosed. *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 20 U.S.P.Q.2d 1746 (Fed. Cir. 1991). Unstated elements in a reference are inherent when they exist as a "matter of scientific fact". *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 7 U.S.P.Q.2d 1057 (Fed. Cir.), *cert. denied*, 488 U.S. 892 (1988) and *Hughes Aircraft Co. v. United States*, 8 U.S.P.Q.2d 1580 (Ct. Cl. 1988). Otherwise, the invention is not inherently anticipated.

In the present case, the step of "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page" is not inherently anticipated by the primary reference because this step is not *necessarily* present. The Examiner believes that the entries contained within a TCE table would result in a valid translation because any other result would be contrary to common sense. However, the Specification indicates at page 16 that prefetched DMA addresses that have not been mapped by the operating system can result in invalid translations and subsequent checkstop errors. Thus, valid DMA address translations based on the entries within the TCE table are only a *possible* result, and not a *necessary* result. A meaningful and viable alterative exists to the Examiner's interpretation of what the reference teaches. Therefore, under the standards of the cases cited above, the step of initializing the entries to be valid is not inherently disclosed by *Dawkins*. For this reason, *Dawkins* does not anticipate claim 1.

Independent claims 10 and 19 are substantially similar to independent claim 1. Therefore, *Dawkins* also does not anticipate independent claims 10 and 19 for at least the reasons set forth above with respect to claim 1. The Examiner, however, asserts that claim 19 is "substantially disclosed" by paragraph 0050. Claim 19 was reproduced in section IV above. Paragraph 0050 and Figure 4 of *Dawkins* are as follows:

> [0050] Those of ordinary skill in the art will appreciate that the hardware and software depicted in FIG. 4 may vary. For example, more or fewer processors and/or more or fewer operating system images may be used than those depicted in FIG. 4. The depicted example is not meant to imply architectural limitations with respect to the present invention.

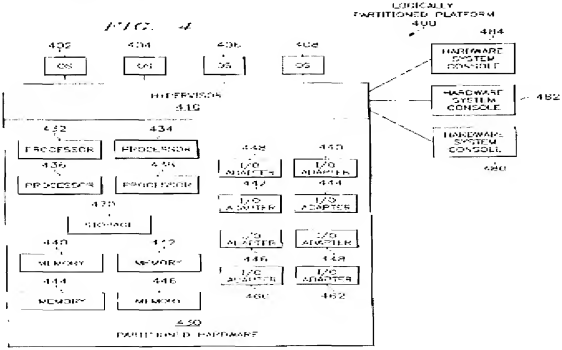


Figure 4 depicts a logically partitioned platform. This depiction and the accompanying description fail to teach a translation control entry table, and the first, second, third, and fourth instructions recited in claim 19. Therefore, *Dawkins* does not anticipate claim 19.

The Examiner also asserts that claim 19 is "substantially disclosed" by paragraph 0051, reproduced below:

> [0051] The present invention provides a method, apparatus, and computer implemented instructions for controlling the power and rebooting logical partitions within a data processing system. The mechanism of the present invention provides functionality to turn off the power to a logical partition or to the entire system. The mechanism also provides for rebooting partitions within the data processing system. In the depicted examples, the physical power switch and reset switch are disabled within the data processing system. This disablement occurs after the data processing system powers up and executes logical partitions. A virtual power switch and virtual reset switch is provided to allow individual partitions to be turned on or off and to allow individual partitions to be rebooted.

Paragraph 0051, however, only describes that the physical power and reset switches of a logically partitioned platform are replaced with virtual power and reset switches. As with paragraph 0050 and Figure 4, paragraph 0051 fails to mention a translation control entry table, and the first, second, third, and fourth instructions recited in claim 19. Thus, *Dawkins* does not anticipate claim 19.

The Examiner also asserts that paragraph 0066 "substantially disclosed" claim 19. Paragraph 0066 is reproduced below:

> [0066] Turning next to FIG. 9, a flowchart of process used for turning off power to a partition is depicted in accordance with a preferred embodiment of the present invention. The process illustrated in FIG. 9 may be implemented as computer instructions executed by service processor 366 in FIG. 3.

Paragraph 0066 only describes the flowchart in Figure 9. Figure 9 is reproduced below:

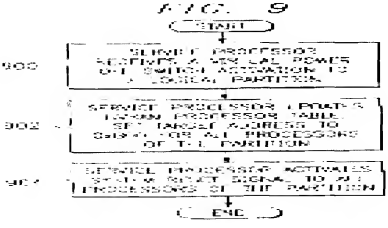
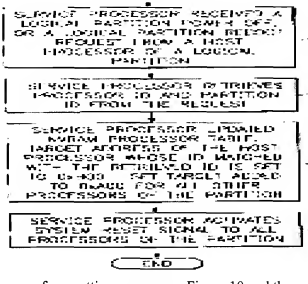


Figure 9 and the accompanying text describe the process used for turning off power to a partition in accordance with the teachings of *Dawkins*. Paragraph 0066 and Figure 9 fail to mention a translation control entry table, and the first, second, third, and fourth instructions recited in claim 19. Thus, *Dawkins* does not anticipate claim 19.

Similarly, paragraph 0068 only indicates that Figure 10 is a flowchart illustrating the process used for resetting processors in accordance with the teachings of *Dawkins*. Figure 10 is reproduced below:

FIG. 10



In depicting the process for resetting processors, Figure 10 and the accompanying text fails to mention a translation control entry table, and the first, second, third, and fourth instructions recited in claim 19. Thus, *Dawkins* does not anticipate claim 19.

The Examiner also alleges that paragraph 0076 "substantially disclosed" claim 19. Paragraph 0076, however, only describes the invention of *Dawkins*. Paragraph 0076 is reproduced below:

> [0076] Thus, the present invention provides an improved method, apparatus, and computer implemented instructions for handling requests to turn off logical partitions and/or reboot logical partitions. The mechanism of the present invention provides an ability to reboot or reset processors assigned to a particular logical partition without rebooting or resetting other processors assigned to other logical partitions in the data processing system. This mechanism allows for handling resources for a logical partition individually without affecting other logical partitions.

Paragraph 0076 indicates only that *Dawkins* is directed toward providing an ability to reboot or reset processors of an individual logical partition without rebooting or resetting the other processors. Paragraph 0076 fails to mention a translation control entry table, and the first, second, third, and fourth instructions recited in claim 19. For this reason, *Dawkins does* not anticipate claim 19.

V.B. Asserted Anticipation of Dependant Claims

Because claims 2, 3, 5, 6, 8, 11, 12, 14, 15, 17, 20, 21, 23, 24, and 26 depend from claims 1, 10, and 19, the same distinctions between *Dawkins* and the inventions recited in claims 1, 10, and 19 apply for these claims. Consequently, Applicants have overcome the rejection of claims 2, 3, 5, 6, 8, 11, 12, 14, 15, 17, 20, 21, 23, 24, and 26.

V.C. Conclusion as to Asserted Anticipation

Applicants have proved that *Dawkins* does not teach all the features of independent claims 1, 10, and 19. Further, because claims 2, 3, 5, 6, 8, 11, 12, 14, 15, 17, 20, 21, 23, 24, and 26 depend from claims 1, 10, and 19, Applicants have also proved that *Dawkins* does not anticipate claims 2, 3, 5, 6, 8, 11, 12, 14, 15, 17, 20, 21, 23, 24, and 26. Therefore, the rejection of claims 1-3, 5, 6, 8, 10-12, 14, 15, 17, 19-21, 23, 24, and 26 has been overcome.

Furthermore, *Dawkins* does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to implement *Dawkins* and "writing the reserved page" and "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid," one of ordinary skill in the art would not be led to modify *Dawkins* to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify *Dawkins* in this manner, the presently claimed invention can be reached only through an improper use of hindsight using Applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

VI. Asserted Obviousness under 35 U.S.C. § 103

The Examiner rejected claims 7, 16, and 25 as obvious over *Dawkins*, in further view of *Tannenbaum et al.*, Operating Systems: Design and Implementation, (1997) (hereinafter "*Tannenbaum*"). Also, the examiner rejected claims 9, 18, and 27 as unpatentable over *Dawkins*. These rejections are respectfully traversed.

The Examiner failed to state *a prima facie* obviousness rejection with respect to dependent claims 7, 9, 16, 18, 25, and 27 because the proposed combination of references does not teach or suggest all the features of independent claims 1, 10, and 19. Furthermore, the Examiner has failed to provide proper motivation to modify or combine the above-cited references.

VI.A. The Cited References Fail to Teach all the Features of the Independent Claims

The Examiner failed to state a *prima facie* obviousness rejection because the proposed combination of the cited references when considered as a whole does not to teach all the features of

independent claims 1, 10, and 19. The Examiner has also failed to state a *prima facie* obviousness rejection of dependent claims 7, 9, 16, 18, 25, and 27 at least by virtue of their dependency on independent claims 1, 10, and 19.

If the Patent Office does not produce a *prima facie* case of unpatentability, then without more Applicants are entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985). A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990).

In section V.A, Applicants proved that *Dawkins* fails to teach "writing the reserved page" and "initializing all entries in the translation control entry table, wherein all entries are initialized to be valid and contain the address of the reserved page." *Tannenbaum* fails to cure the deficiencies of *Dawkins* because *Tannenbaum* also does not teach or suggest the above-referenced features of claims 1, 10, and 19. The examiner does not assert otherwise. Instead, *Tannenbaum* teaches equipping computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table, which is wholly unrelated to these claimed features. Consequently, the Examiner has failed to state a *prima facie* obviousness rejection with respect to claims 7, 9, 16, 18, 25, and 27.

VI.B. *Dawkins* and *Tannenbaum* Would Not Be Combined By One of Ordinary Skill in the Art Because They Address Different Problems

Regarding a teaching, suggestion, or motivation to combine the references the examiner states that:

> **Per claims 7, 16 and 25**, Dawkins does not specifically teach setting all valid bits to "1". However, Tannenbaum teaches an address translation mechanism (TLB, see Tannenbaum, Pg. 328, Fig. 4-12) that sets valid bits of its table entries to "1" to indicate the entries are valid (in use, see Pg. 328, Ln. 20-21). Since Dawkins initializes its TCE table entries to contain the address of the reserved page as described in claim 1, the entries are in use and therefore valid. Hence, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to associate valid bits to the table entries and set the bits to "1" to indicate that the entries are valid (in use).

Office Action dated June 6, 2006, p. 6.

However, one of ordinary skill would not combine the references to achieve the invention of claim 1 because the references are directed towards solving different problems. It is necessary to consider the reality of the circumstances--in other words, common sense--in deciding in which fields a person of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor. *In re Oetiker*, 977 F.2d 1443 (Fed. Cir. 1992); *In re Wood*, 599 F.2d 1032, 1036, 202 U.S.P.Q. 171, 174 (CCPA 1979). In the case at hand, the cited references address distinct problems. Thus, no common sense reason exists to establish that one of ordinary skill would reasonably be expected to look for a solution to the problem facing the inventor. Accordingly, no teaching, suggestion, or motivation exists to combine the references and the Examiner has failed to state a *prima facie* obviousness rejection of claim 1.

Tannenbaum is directed to the problem of equipping computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table. *Tannenbaum*, when viewed as a whole, sets forth a solution "*to equip computers with a small hardware device* for mapping virtual addresses to physical addresses *without going through the page table.*" (*Tannenbaum*, p.328, lines 11-13.) To this end, *Tannenbaum* teaches the use of a Translation Lookaside Buffer.

In stark contrast, *Dawkins* is directed to solving the problem of turning power on and off in a data processing system. For example, *Dawkins* provides that:

> [0006] The configuration of these different partitions are typically managed through a terminal, such as a hardware system console (HSC). These terminals use objects, also referred to as profiles that are defined and modified in HSC. The profiles are used to configure LPARs within the data processing system. Multiple HSCs may be present and used for maintaining and configuring LPARs in the data processing system. These profiles used to configure the data processing system in LPARs are often required to be accessible to any HSC that is in communication with the data processing system. Maintaining profiles between these HSCs are often difficult and require processes for maintaining synchronization of the profiles at each HSC. Therefore, it would be advantageous to have improved method, apparatus, and computer implemented instructions for maintaining profiles for different HSCs.
>
> [0007] With multiple partitions executing at the same time, a command to reset the data processing system will reset all the partitions. Similarly, pressing a reset button on the data processing system also will cause all of the partitions to reset. Further, turning off the power to the system may result in errors if all of the logical partitions have not been properly shut down. With these situations, the physical buttons for power and reset on a computer should not be used in a system using logical partitions.

> [0008] Therefore, it would be advantageous to have an improved method and apparatus for resetting and/or turning off power to a data processing system..

Dawkins, paragraphs 0006-0008.

Based on the plain disclosures of the references themselves, the references address completely distinct problems that are unrelated to each other. The problem of equipping computers with a small hardware device for mapping virtual addresses to physical addresses without going through the page table is completely distinct from the problem of turning power on and off in a data processing system. Because the references address completely distinct problems, one of ordinary skill would have no reason to combine or otherwise modify the references to achieve the claimed invention. Thus, one of ordinary skill in the art would not combine these references to achieve the claimed inventions because no teaching, suggestion, or motivation exists to combine the references in the manner suggested by the Examiner. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against the claims.

VI.C. The Examiner Must Have Used Impermissible Hindsight When Fashioning the Rejections

In addition, the Examiner's has failed to state a *prima facie* obviousness rejection against the claims because the Examiner used impermissible hindsight when fashioning the rejection. Personal opinion cannot be substituted for what the prior art teaches because a *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). Additionally, "[i]t is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986).

In this case, the references address starkly different problems, as shown above. Additionally, the references do not teach what the Examiner asserts the references to teach. Therefore, the Examiner could only have fashioned the rejections by using the Examiner's personal opinion or by picking and choosing features from starkly different references. The rejection appears to be based on "keyword searches" and establishment of the existence of terms, rather than on a fair evaluation of the teachings of the references as a whole. Accordingly, the Examiner must have used impermissible hindsight when fashioning the rejections. Accordingly, under the standards of *In re Bell* and *In re Hedges*, the Examiner failed to state a *prima facie* obviousness rejection of the claims.

The Examiner cites page 328, lines 20 and 21 of *Tannenbaum* in support of the above-referenced rejection: "Another bit indicates whether the entry is valid (i.e., in use) or not." However, *Tannenbaum*, when viewed as a whole, sets forth a solution "*to equip computers with a small hardware device* for

mapping virtual addresses to physical addresses *without going through the page table*." (*Tannenbaum*, p.328, lines 11-13.) To this end, *Tannenbaum* teaches the use of a Translation Lookaside Buffer. In contrast, *Dawkins* teaches that memory is mapped for a DMA operation by means of a *TCE page table stored in the memory*. (*See*, e.g., *Dawkins*, paragraphs 0043-46.) Thus, in view of *Tannenbaum's* teaching, one of ordinary skill would be motivated to avoid combining the small hardware device of *Tannenbaum* with *Dawkins* because *Dawkins* already teaches a solution for mapping a DMA operation.

Further, *Dawkins* teaches that the DMA mapping is performed by means of a TCE page table stored in system memory. Thus, *Dawkins* would have no need for *Tannenbaum's* extraneous hardware device to accomplish the DMA mapping that *Dawkins* teaches by means of the page table stored in memory. For this reason, one of ordinary skill in the art would be motivated against combining *Dawkins* and *Tannenbaum*.

Given that one of ordinary skill would be motivated against combining the references and given that no need exists to combine the references, the only logical conclusion to draw is that the Examiner must have used personal opinion and picked and chosen features from the references. Doing so constitutes impermissible hindsight.

Based on the plain disclosures in the references, the only suggestion to modify the references is found in Applicants' specification. Hence, the Examiner must have used Applicants' specification to find a teaching, suggestion, or motivation to combine the references. Combining the references in this manner constitutes impermissible hindsight and fails to comport with the standards of *Graham v. John Deere Co.*, 383 U.S. 1 (1966), which requires a proper teaching, suggestion, or motivation to combine or modify references to achieve a proper obviousness rejection. Accordingly, the Examiner has failed to state a *prima facie* obviousness rejection against claim 1.

VI.D. The Proposed Combination When Considered as a Whole Does Not Teach all of the Features of Claims 9, 18, and 27

With respect to claims 9, 18, and 27, the Examiner has also failed to state a proper motivation to modify *Dawkins* or combine *Dawkins* with *Tannenbaum*. The Examiner states:

> **Claims 9, 18 and 27** are rejected under 35 U.S.C. §103(a) as being unpatentable over Dawkins. Per claims 9, 18 and 27, Dawkins does not specifically teach the size of the TCE table, the number of table entries, or the size of the table entries. However, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that these specific values are dictated by design choices and system parameters such as the size of system memory, page size, addressing format and performance costs.

Office Action dated June 6, 2006, pp. 6-7.

Dawkins does not teach or suggest the features wherein the translation control entry table comprises a 2MB TCE table having 512K 4-byte entries as recited in claim 9. The Examiner states only that "design choice" and "system parameters" would render obvious the TCE table size and TCE table entry size recited in claims 9, 18, and 27. However, "design choice" and "system parameters" appear to be offered as a substitute for a proper teaching, suggestion, or motivation to combine or modify the references. Such outdated maxims are improper substitutes for a proper teaching, suggestion, or motivation to modify or combine references under the mandated test for patentability set forth in *Graham v. John Deere Co.*, 383 U.S. 1 (1966).

Additionally, in light of the fact that *Dawkins* does not provide support for the Examiner's assertion, the Examiner's rejection is without adequate basis. If, however, the Examiner is relying upon personal knowledge, then Applicants respectfully request the Examiner to submit an affidavit pursuant to 37 C.F.R. 1.104(d)(2) setting forth specific factual statements and explanations in support the Examiner's findings relating to the obviousness rejection of claims 9, 18, and 27.

VII. Conclusion

For the above-stated reasons, the subject application is patentable over *Dawkins* and *Tannenbaum* and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: September 1, 2006

Respectfully submitted,

/Theodore D. Fay III/

Theodore D. Fay
Reg. No. 48,504
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants

TF/SL